



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,326	11/04/2003	Cheol Ho Joh	CU-3430 RJS	4928
26530	7590	12/23/2005	EXAMINER	
LADAS & PARRY LLP 224 SOUTH MICHIGAN AVENUE SUITE 1600 CHICAGO, IL 60604			MATISIAK, JENNIFER E	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/701,326	JOH ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Jennifer Matisiak	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3,6-8 is/are rejected.
- 7) ☒ Claim(s) 4 and 5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. The term "relatively small thickness" in claim 8 is a relative term which renders the claim indefinite. The term "relatively small thickness" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Additionally, it is not known whether the thickness is small relative to the lead frame or the die of the device of the instant invention.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 3, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 20020153599), hereinafter Chang, in further view of Kim et al. (US 20030011052), hereinafter Kim.

Regarding claim 1, Chang discloses a chip-stacked package (Fig. 2, for example) comprising: a doubly down-set lead frame (23 of Fig. 2) having down-set tip to be wire-bonded (231 of Fig. 2); a first semiconductor chip (21 of Fig. 2) attached under the down-set tip of the lead frame; a first metal wire (26 of Fig. 2) electrically connecting bonding pads (para [0005], for example) of the first semiconductor chip with the down-set tip of the lead frame; a second semiconductor chip (22 of Fig. 2) attached on the lead frame; a second metal wire (27 of Fig. 2) electrically connecting the second semiconductor chip with the lead frame; and a molding compound (28 of Fig. 2) encapsulating the first and second semiconductor chips, the first and second metal wires, and portion of the lead frame. Chang does not disclose "an epoxy molding compound" nor "while exposing the backside of the first semiconductor chip." Kim discloses a semiconductor chip (30 of Fig. 4e, for example) wherein the encapsulant is an epoxy (70 of Fig. 4e, para [0031]) and wherein the backside (36 of Fig. 4e) of the semiconductor chip is exposed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chang by using an epoxy as an encapsulant since it is well known in the art that epoxy is the primary molding compound in electronics packaging. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chang by exposing the backside of the first semiconductor chip since it is

desirable to minimize the total thickness of a package by reducing the size of the molding body.

Regarding claim 2, Chang discloses a first semiconductor chip attached by means of an LOC tape (24 of Fig. 2).

Regarding claim 3, Chang discloses a second semiconductor chip attached by means of adhesives (25 of Fig. 2).

Regarding claim 6, Chang in further view of Kim discloses a chip-stacked package of claim 1. Additionally, Chang discloses a second semiconductor chip is attached by means of an adhesive tape (25 of Fig. 2).

Regarding claim 8, Chang in further of Kim discloses a chip-stacked package of the instant invention (Fig. 2 for example) comprising: down-set lead frame (23 of Fig. 2) having a tip to be wire-bonded, the tip being designed in such manner as to have a relatively small thickness (231 of Fig. 2); a first semiconductor chip attached under the tip of the lead frame (21 of Fig. 2); a first metal wire (26 of Fig. 2) electrically connecting bonding pads (para [0005], for example) of the first semiconductor chip with the tip of the lead frame; a second semiconductor chip (22 of Fig. 2) attached on the lead frame; a second metal wire (27 of Fig. 2) electrically connecting the second semiconductor chip with the lead frame; and a molding compound (28 of Fig. 2, para [0031]) encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the lead frame. Chang does not disclose "an epoxy molding compound" nor "while exposing the backside of the first semiconductor chip." Kim discloses a semiconductor chip (30 of Fig. 4e, for example) wherein the encapsulant is an epoxy

molding compound (70 of Fig. 4e) and wherein the backside (36 of Fig. 4e) of the semiconductor chip is exposed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chang by using an epoxy as an encapsulant since it is well known in the art that epoxy is the primary molding compound in electronics packaging. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chang by exposing the backside of the first semiconductor chip since it is desirable to minimize the total thickness of a package by reducing the size of the molding body.

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, in further view of Kim and Smith et al. (US 2004/0065945), hereinafter Smith.

Regarding claim 7, Chang discloses a chip-stacked package comprising: doubly down-set lead frame (23 of Fig. 2) having a down-set tip to be wire-bonded (231 of Fig. 2); a first semiconductor chip attached under the tip of the lead frame (21 of Fig. 2); a first metal wire (26 of Fig. 2) electrically connecting bonding pads (para [0005]) of the first semiconductor chip with the tip of the lead frame; a second semiconductor chip (22 of Fig. 2) attached on the lead frame; a second metal wire (27 of Fig. 2) electrically connecting the second semiconductor chip with the lead frame; and a molding compound (28 of Fig. 2, para [0031]) encapsulating the first and second semiconductor chips, the first and second metal wires, and a portion of the lead frame. Chang does not disclose "an epoxy molding compound" nor "while exposing the backside of the first

semiconductor chip.” Kim discloses a semiconductor chip (30 of Fig. 4e, for example) wherein the encapsulant is an epoxy molding compound (70 of Fig. 4e) and wherein the backside (36 of Fig. 4e) of the semiconductor chip is exposed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chang by using an epoxy as an encapsulant since it is well known in the art that epoxy is the primary molding compound in electronics packaging. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chang by exposing the backside of the first semiconductor chip since it is desirable to minimize the total thickness of a package by reducing the size of the molding body.

Furthermore, Chang does not disclose “by means of a B-stage material.” Smith discloses a semiconductor chip (32 of Fig. 2E, for example) attached under a lead frame (30 of Fig. 2E) by means of a B stage material (42 of Fig. 2E, para [0050]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Chang by attaching the first semiconductor chip under the lead frame by means of B stage material since it is desirable to attach semiconductor chips to an electronic package before curing the package.

#### ***Allowable Subject Matter***

4. Claims 4 and 5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Matisiak whose telephone number is 571-272-2639. The examiner can normally be reached on Business Days 9:30a-6:30p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 517-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEM

  
Primary Examiner  
Douglas W. Owens